ABSTRACT

A power-on reset circuit for generating a reset signal for an associated IC device includes a pull-up resistor connected between a supply voltage and a tracking node, a pull-down transistor connected between the tracking node and ground potential, and a voltage divider circuit connected between the supply voltage and ground potential. The voltage divider circuit has a first ratioed voltage node coupled to the gate of the pull-down transistor. For some embodiments, the voltage divider circuit includes a first resistor connected between the voltage supply and the first ratioed voltage node, a second resistor connected between the first ratioed voltage node and a second ratioed voltage node, a third resistor connected between the second ratioed voltage node and ground potential, and a shunt transistor connected between the second ratioed voltage node and ground potential has a gate responsive to the reset signal.